Experiment 1

**Aim**: To Perform DC and Transient Analysis of Resistive Load Inverter Circuit

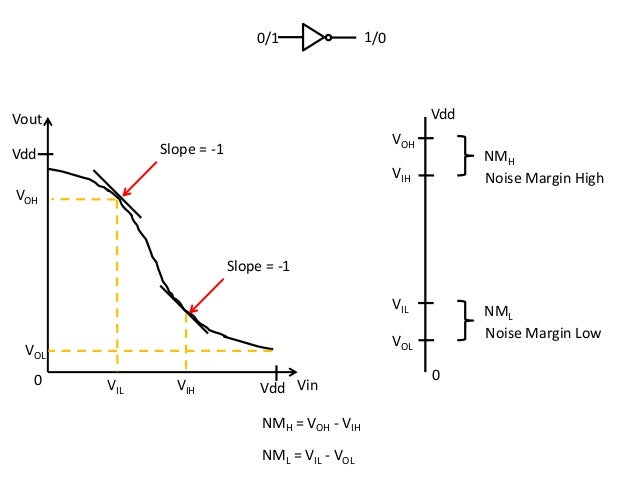
Or

To plot the VTC Curve of Resistive Load Inverter Circuit Tool Used: LTSPICE

Theory:

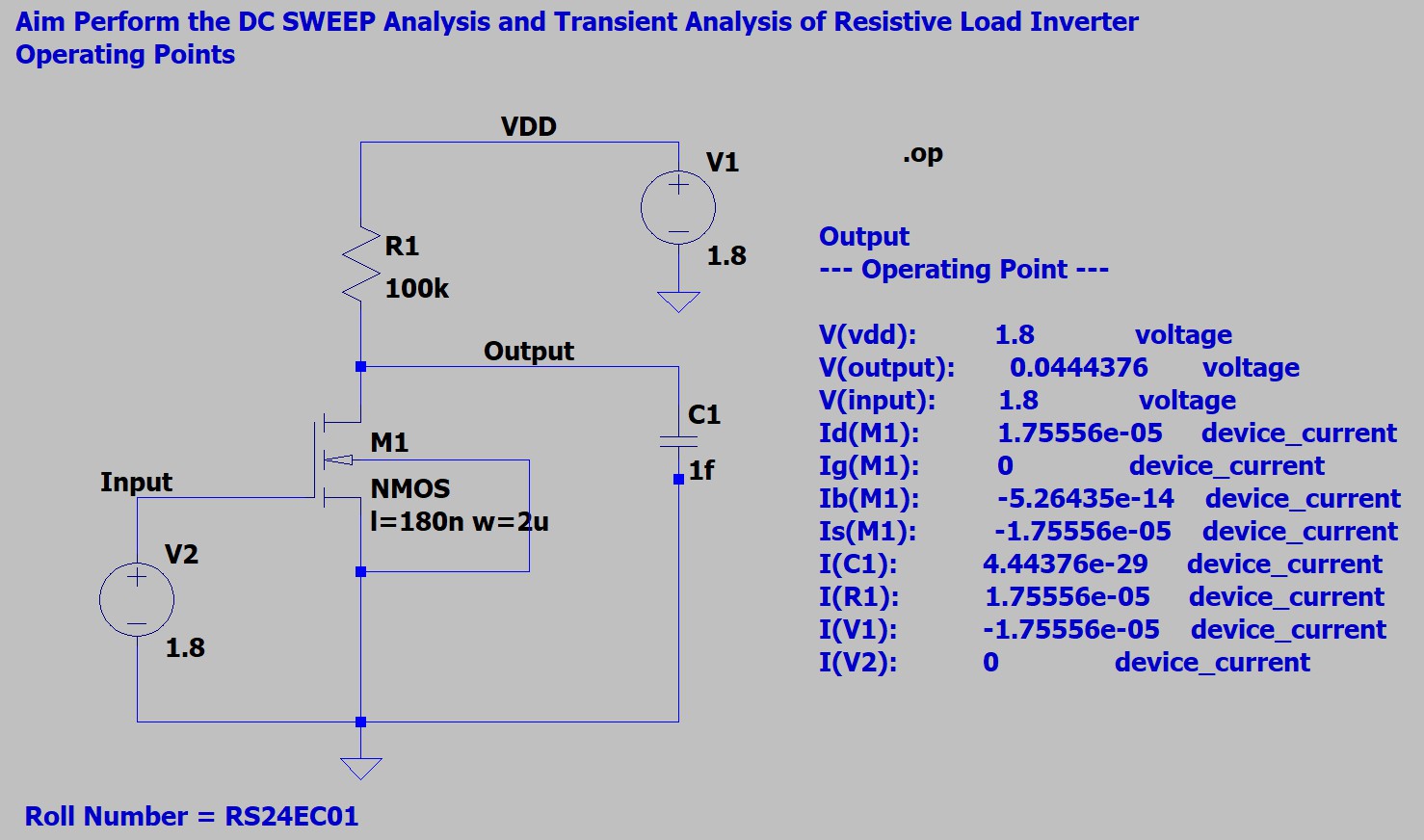
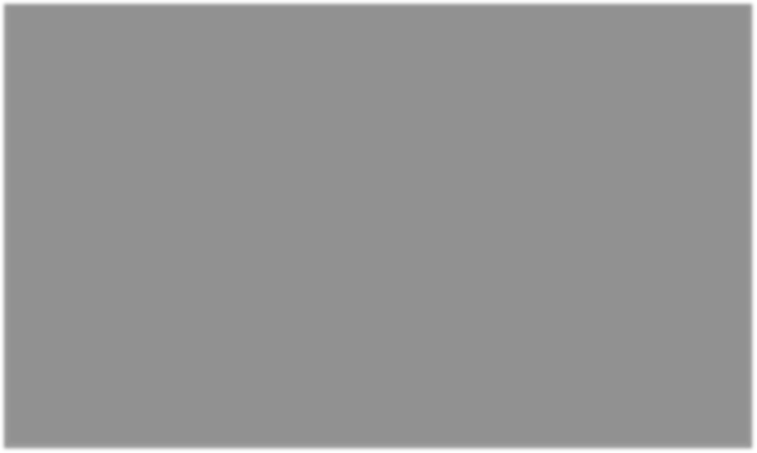
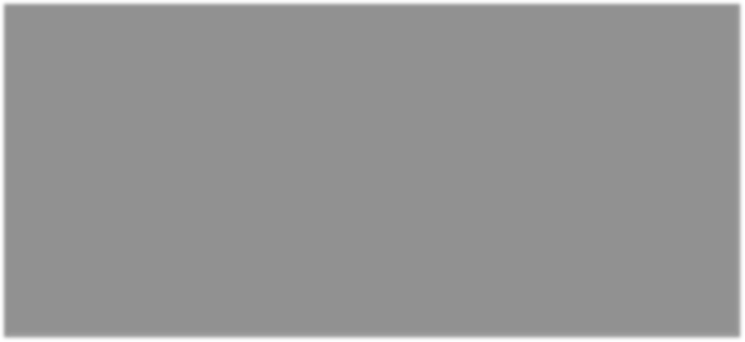
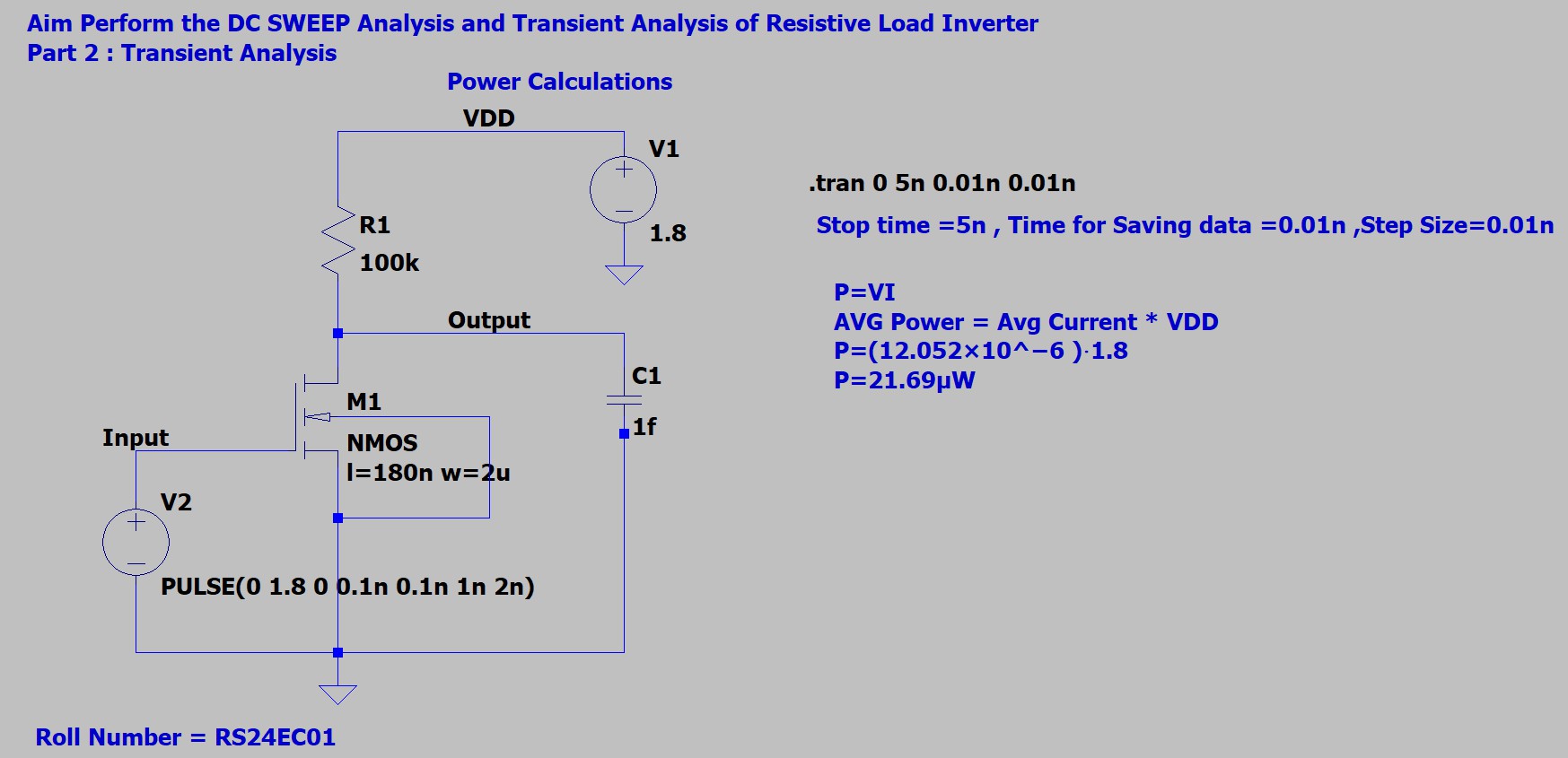
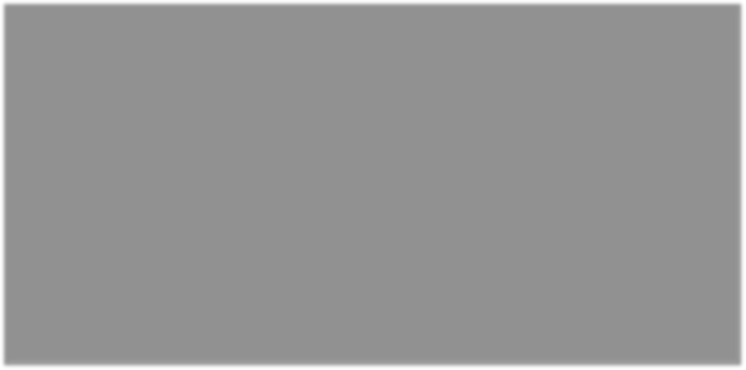
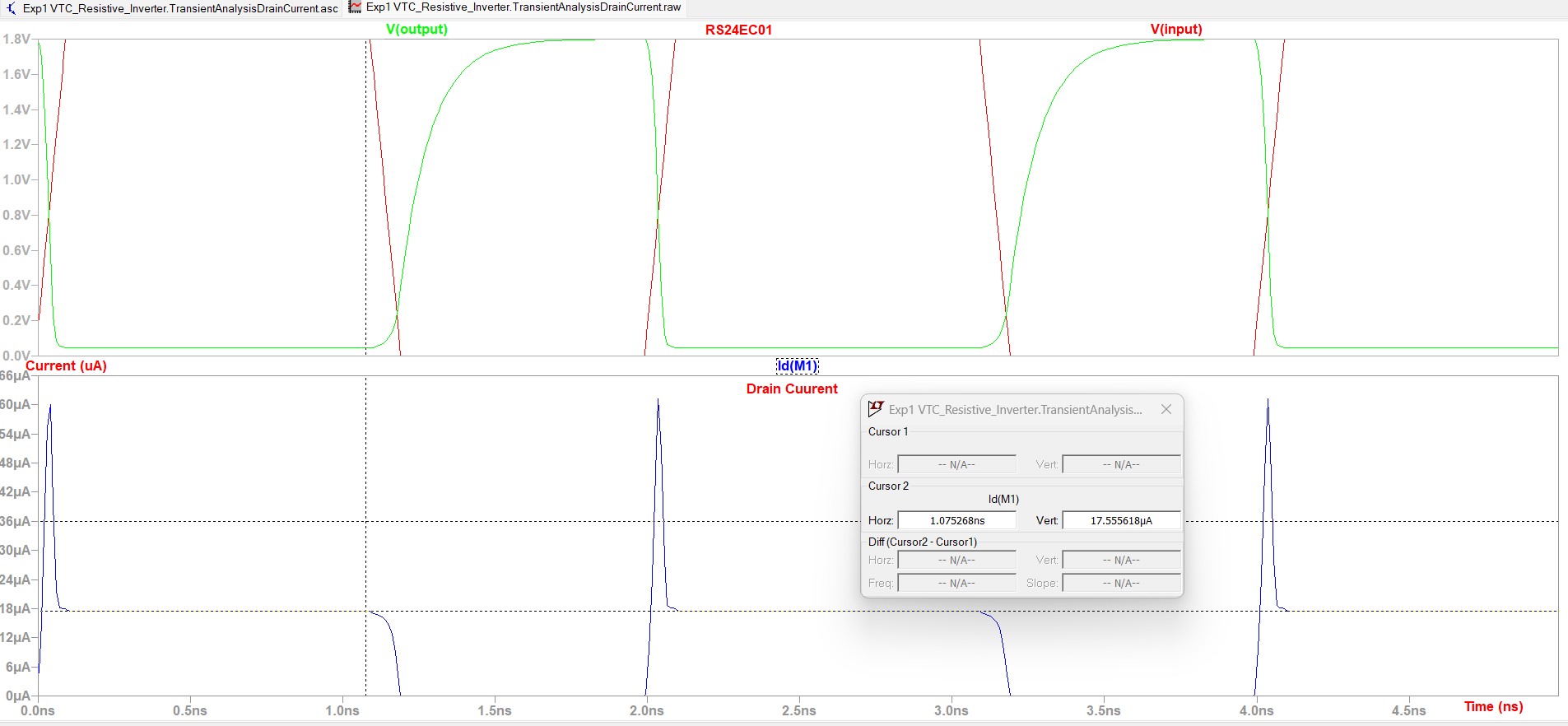
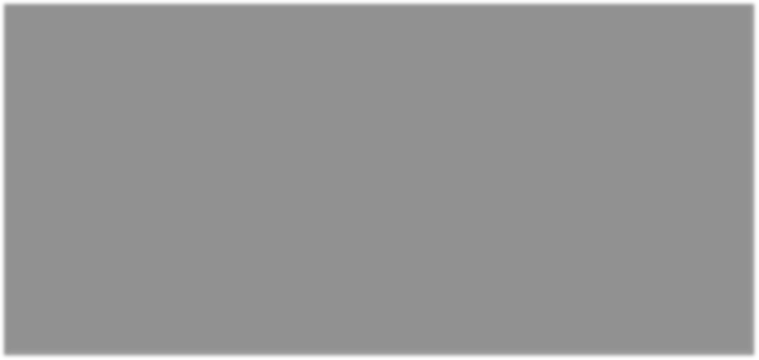
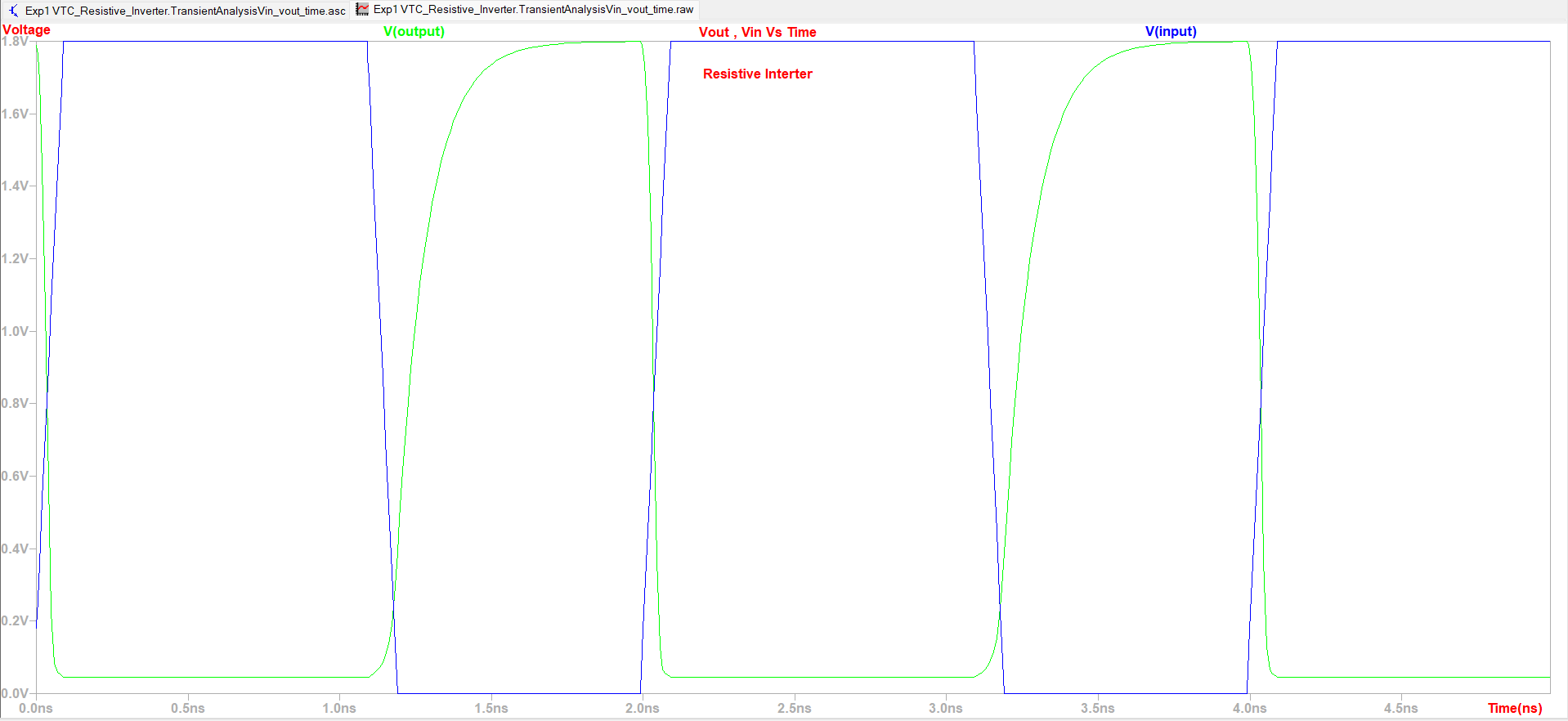
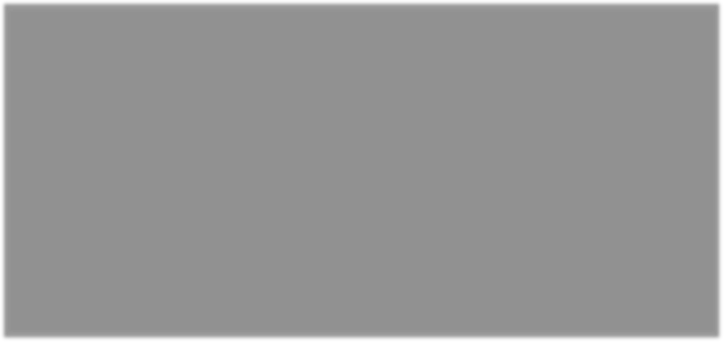
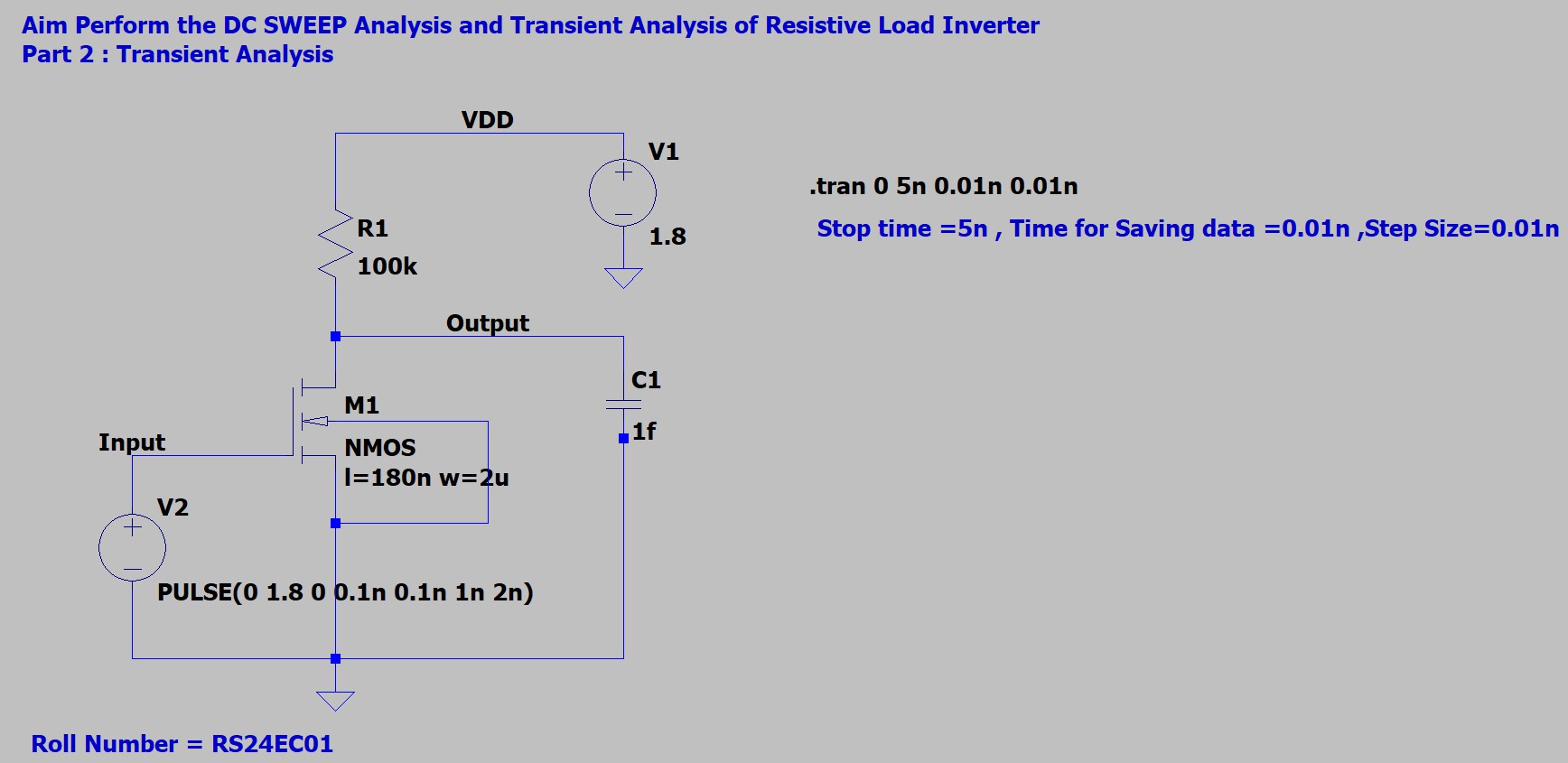
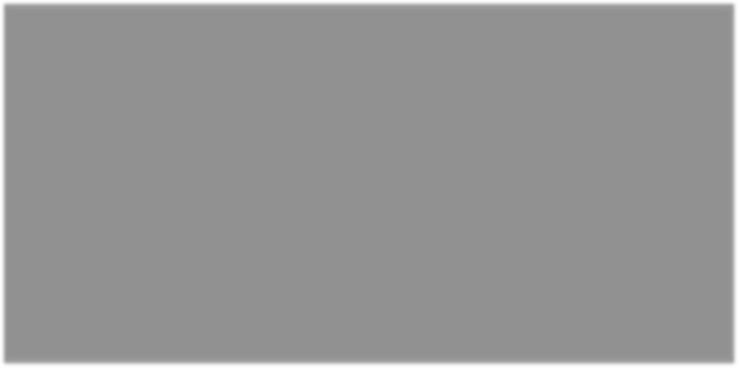
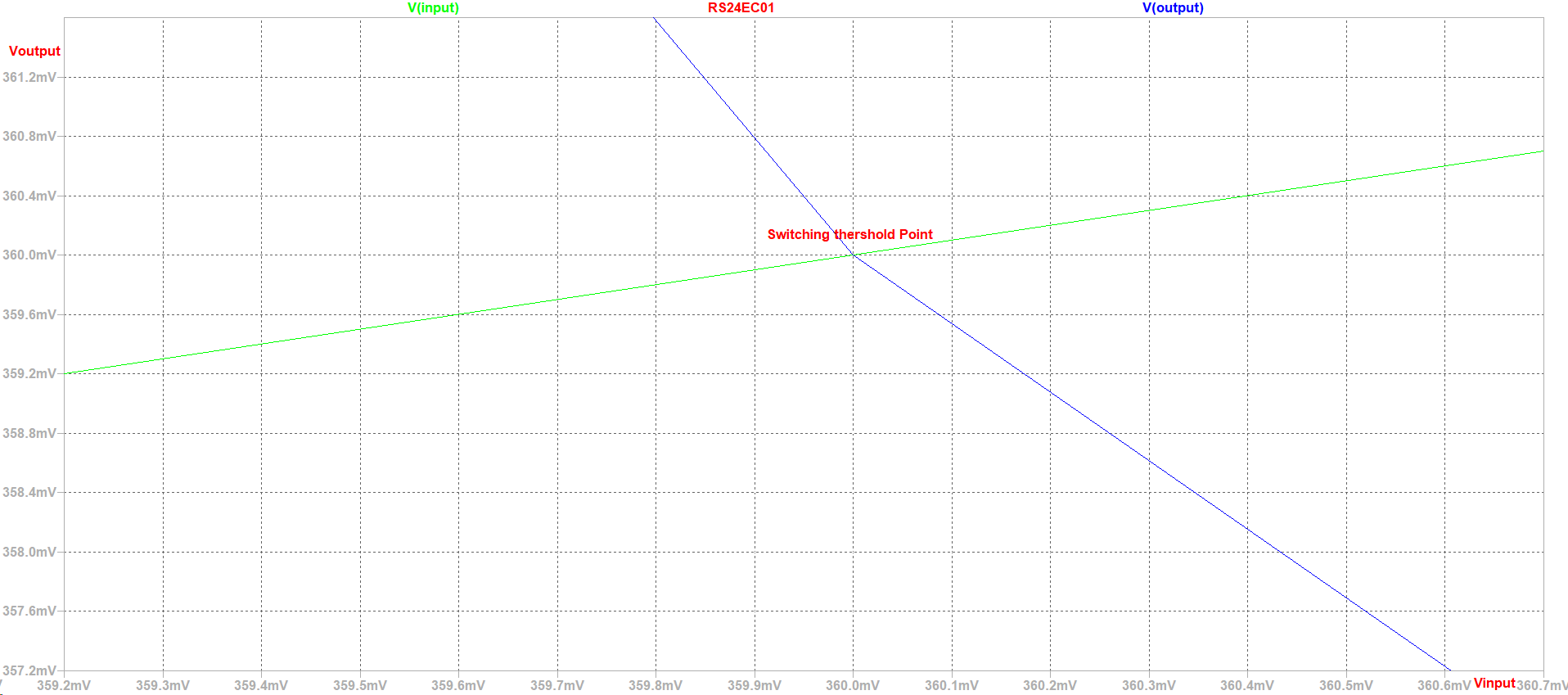
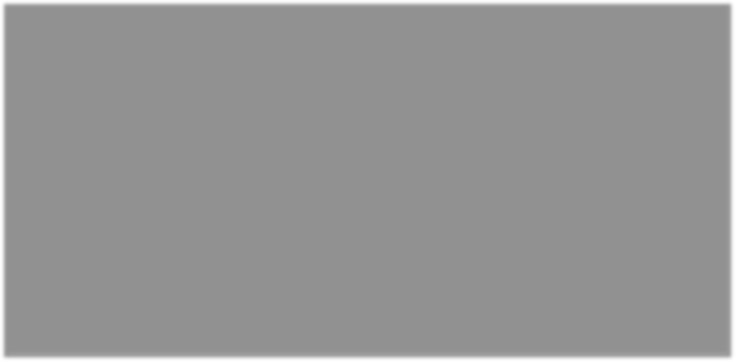
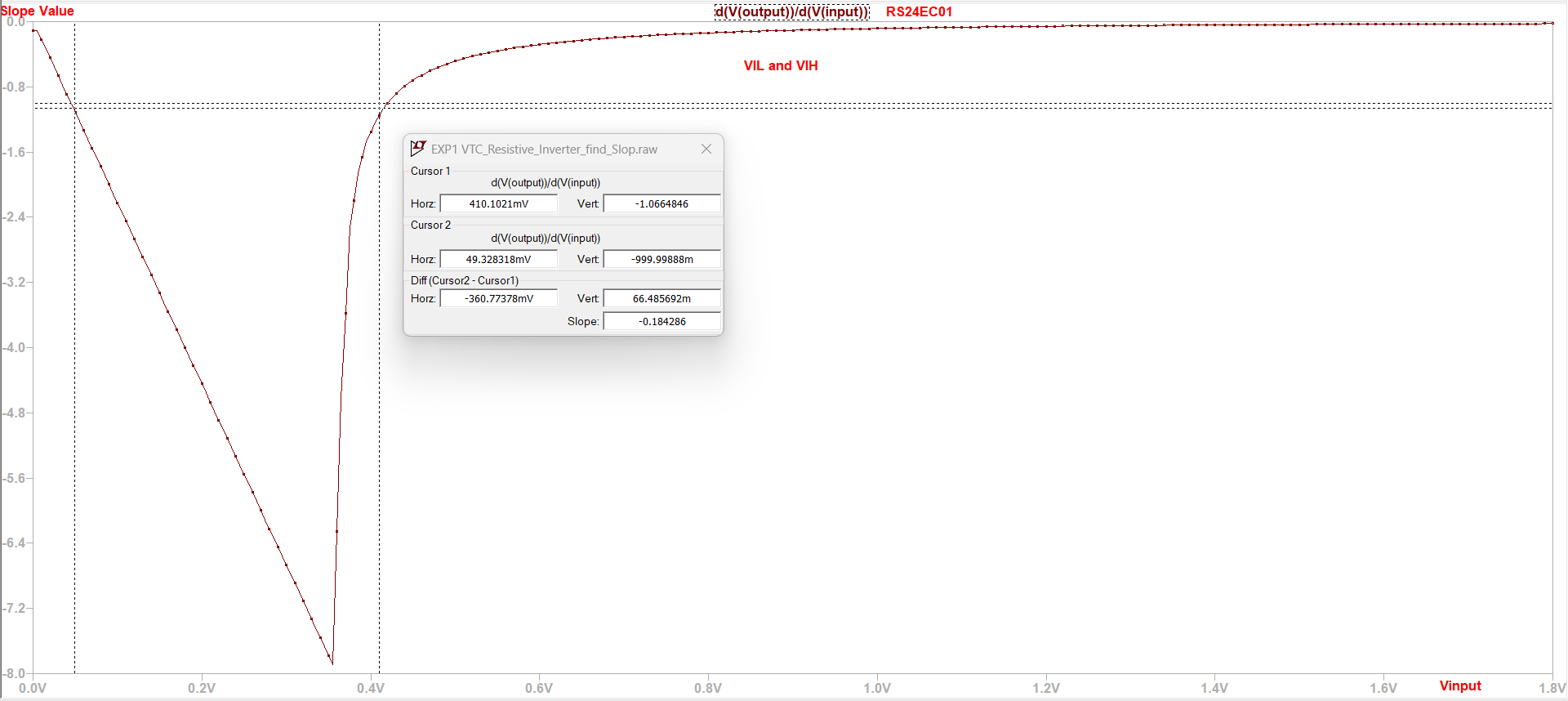
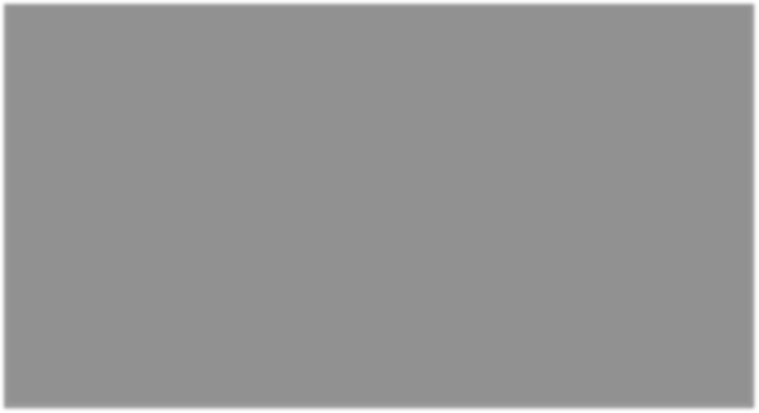
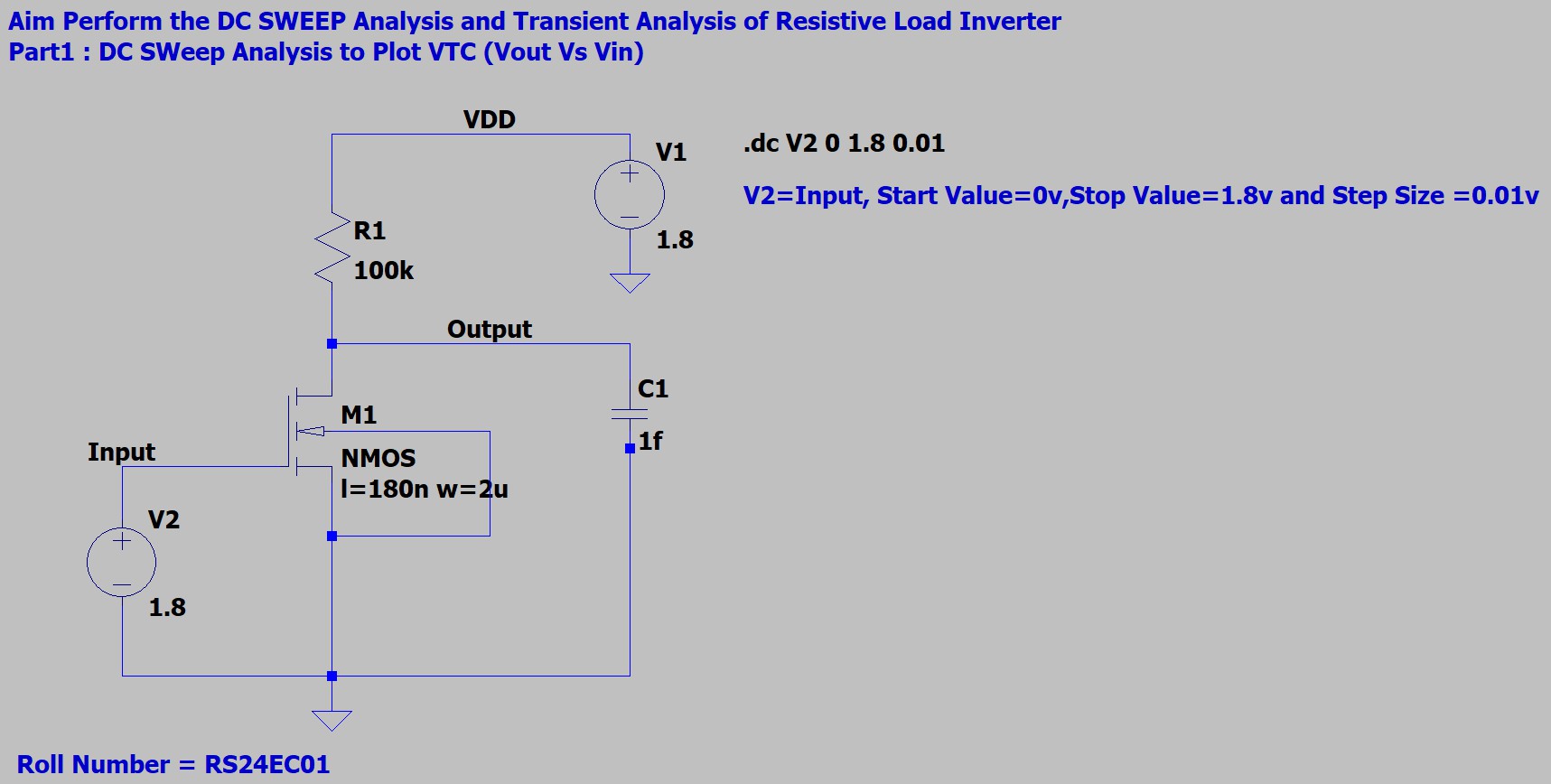
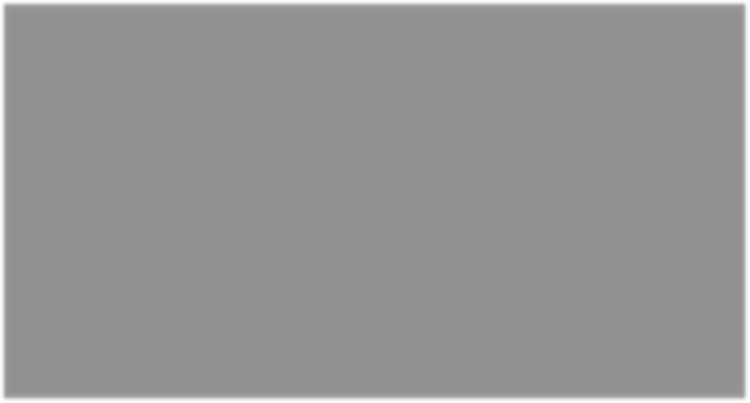
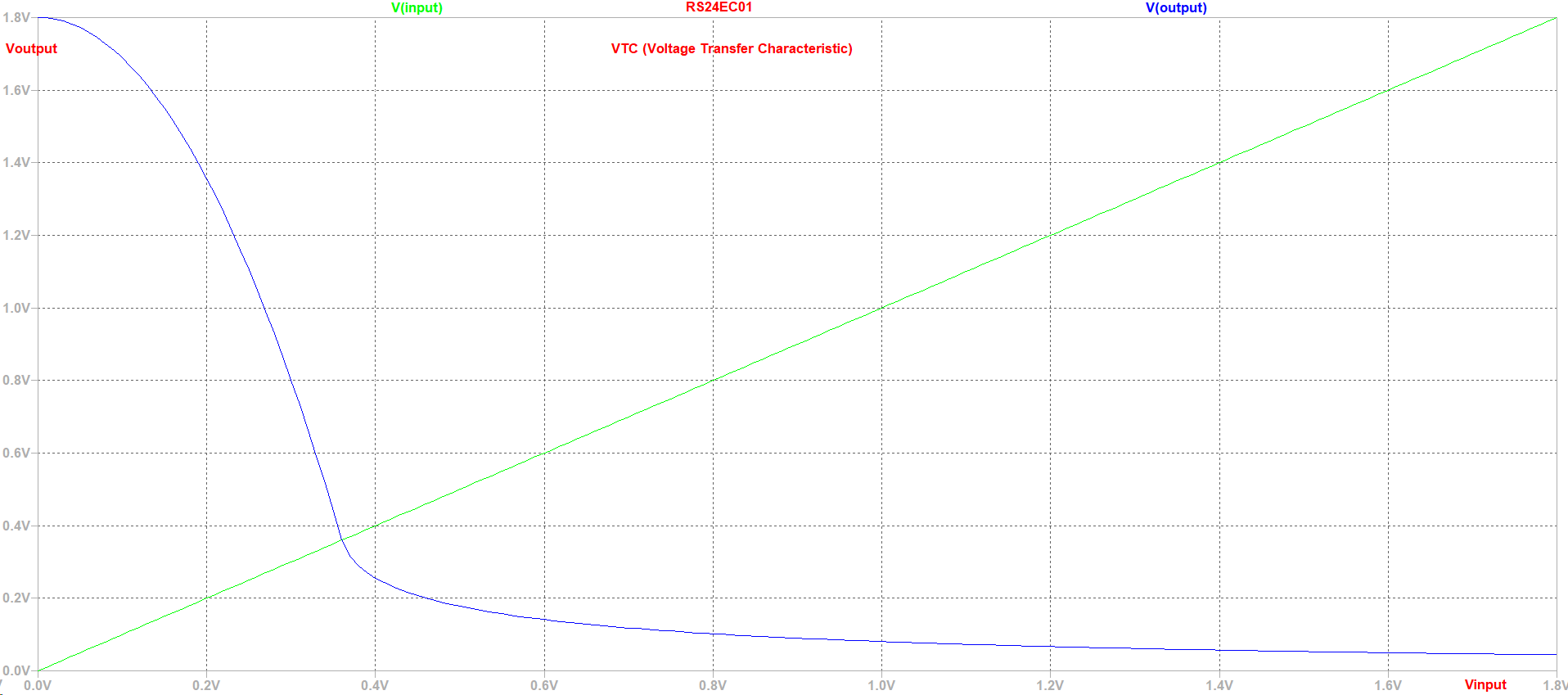
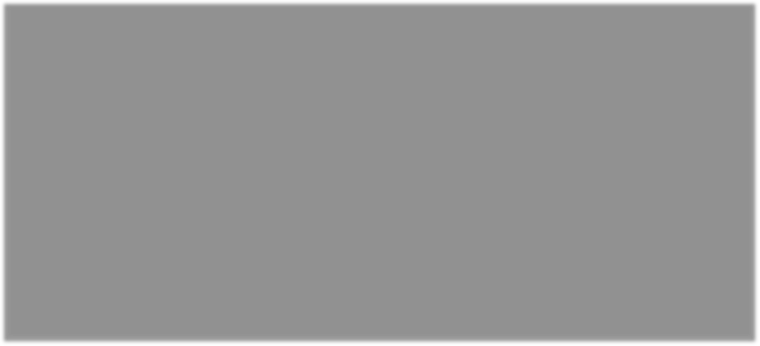
Theory

|  |  |
| --- | --- |
| VIL | Input Low Voltage |
|  | Any voltage between 0 and VIL treated as Logic Zero |
| VOH | Output High Voltage |
|  | Any output voltage level between VOH and VDD treated as Logic One |
| VIH | Input High Voltage |
|  | Any Input voltage level between VIH and VDD will be treated as Logic One |
| VOL | Output Low Voltage |
|  | Any output voltage level between Zero and VOL treated as Logic Zero |

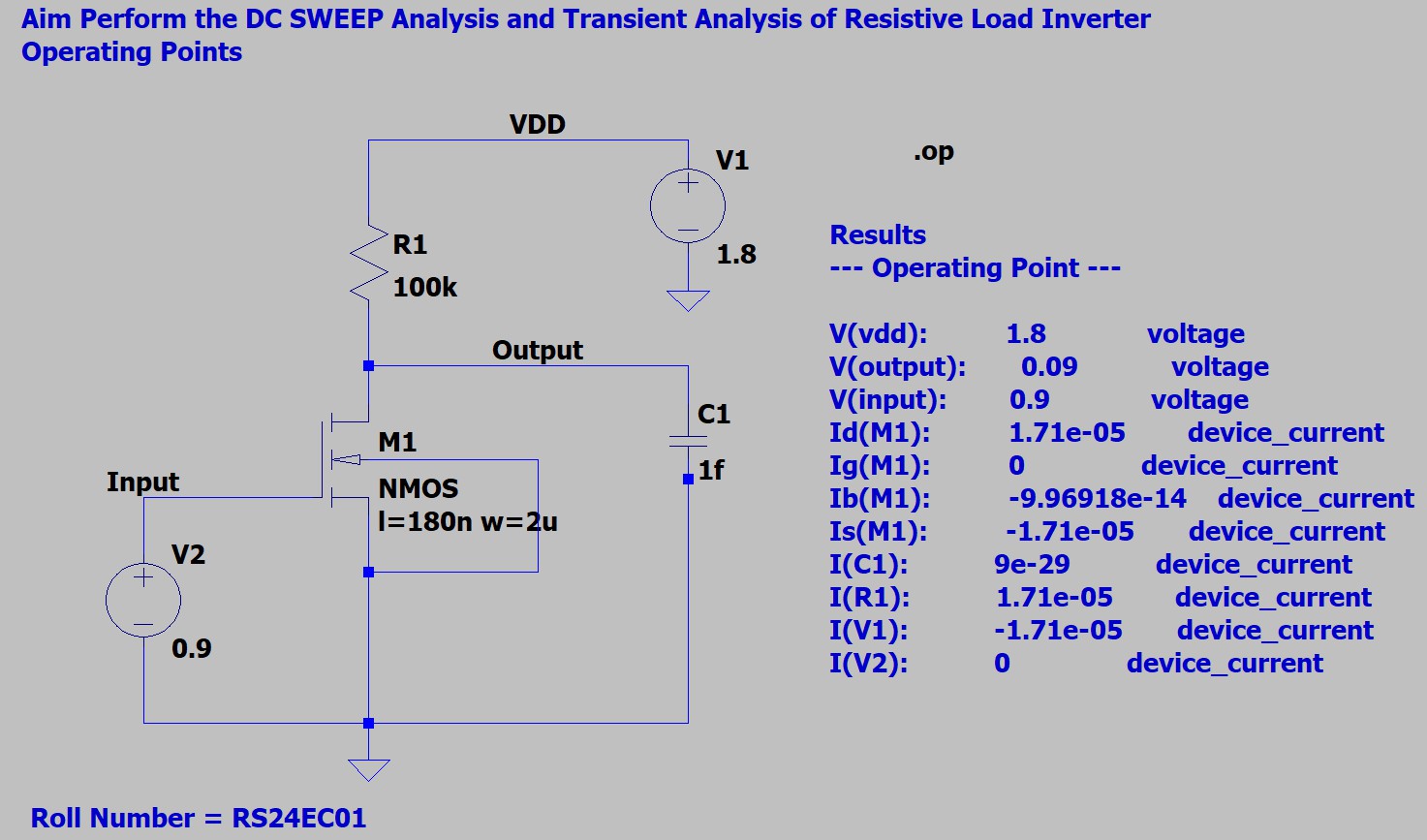
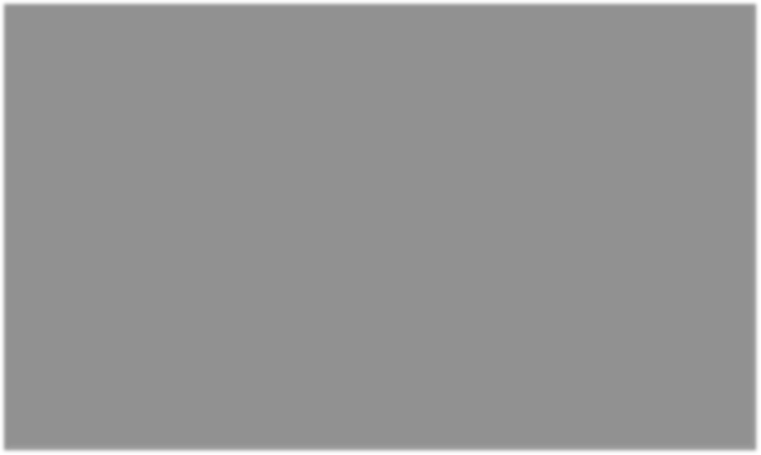


Switching Threshold: A point at which Vin = Vout at this point PMOS and NMOS both are in saturation state both transistors are on. High chances of leakage current flow.

Simulation



**Results**



|  |  |  |
| --- | --- | --- |
| **Parameters** | **Value in mv** | **Value in Volt** |
| VIL | 49.328318mV | 0.049328318 V |
| VIH | 410.1021mV | 0.4101021 V |
| VOL | 44.437587mV | 0.044437587 V |
| VOH | 1.8v | 1.8 V |
| Vm | 360 mV |  |
| **Trans Analysis** | | |
| Id | 17.555365µA |  |
| **Power Calculations** | | |
| Avg Current | 12.052µA |  |
| Avg Power P= VI | 21.69μW |  |